

ABSTRACT OF THE DISCLOSURE

A delay time adjusting circuit adjusts a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other. The circuit comprises first dividing means for dividing a frequency of the input signal by a first frequency division rate; delaying means for delaying the input signal by a predetermined time; second dividing means for dividing a frequency of the input signal delayed by the delaying means by a second frequency division rate; comparing means for comparing a phase of a signal generated by the first dividing means and a phase of a signal generated by the second dividing means; and adjusting means for adjusting the predetermined time according to a comparison result obtained by the comparing means.

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